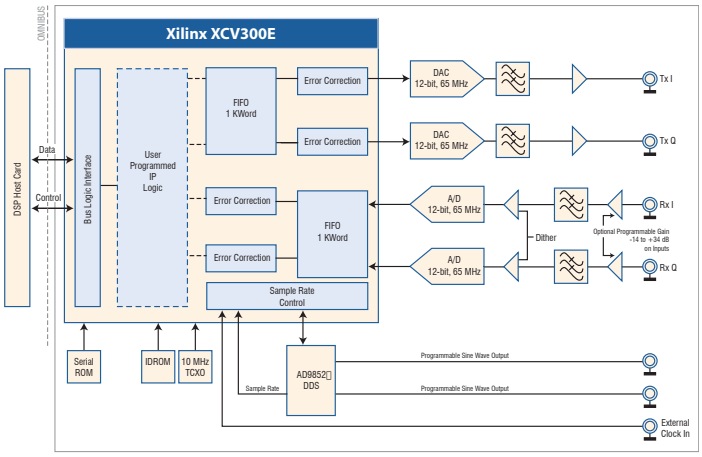
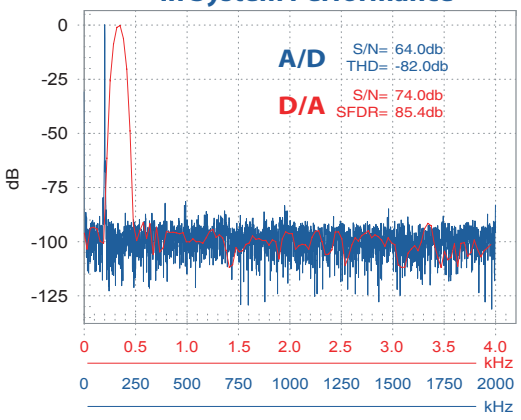
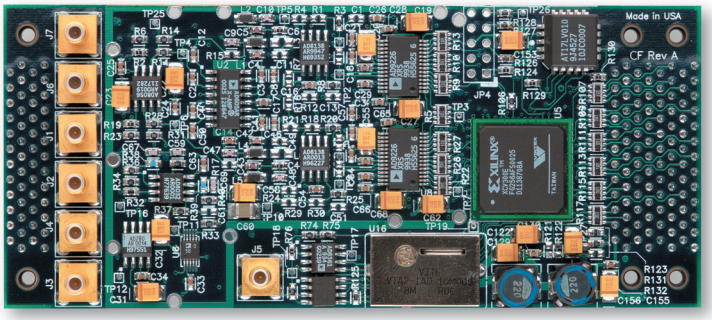
Bus type	Compatible with all OMNIBUS host products Consumes one interrupt to host
Power Requirements	2W
Physicals	OMNIBUS mezzanine card; 2.0" x 4.6"
A/D Converters	2 Analog Devices AD9226 converters
Resolution	12-bit
Update Rate	65 MHz max.
Analog Input Range	±1V at 0dB; +40dB with programmable gain amplifier
Analog Input type	Single ended to 50 Ohm SMB connector
Analog Input Impedance	50 Ohm
Input Filter Characteristics	Lowpass or Bandpass 7 pole; -3 dB point @12 MHz May be bypassed for DC inputs
SNR	>64 dB (without variable gain); >53 dB (with variable gain)
SINAD	45 dB (with variable gain)
THD	<0.01%
Conversion Trigger Sources	On board DDS or External clock Optional dither on A/D for improved S/N
Interface to Host Card	Memory mapped configurable 32-bit result Programmable Xilinx XCV300E FPGA
D/A converter	Analog Devices AD9765 converters
Resolution	12-bit
Output Range	±1V
Settling Time	35 ns
Dynamic Range	72dB
THD	0.01%
Offset Error	Software controlled digital trimming on each channel - factory calibrated
Gain Error	Software controlled digital trimming on each channel - factory calibrated
Interface to DSP	Memory mapped 32 bit result, programmable via Xilinx XCV300E FPGA
DDS - AD9852	200 MHz input with 40 bit resolution in frequency max. Maximum DDS output rate is 80 MHz
TCXO	5 ppm TCXO (10 MHz) onboard



In System Performance





CF - High-Speed Analog I/O with FPGA for Custom Firmware

The CF module is an excellent platform to develop signal processing in firmware, either for the validation of new IP logic algorithms using real-world signals, or for the fast pre-processing of signals in a high-speed data acquisition system. Much more than a bare-bone development kit, the CF is a complete, scalable solution combining a Xilinx XCV300E FPGA with two 12-bit analog I/O channels clocked up to 65MHz and a bus interface to a DSP. The CF module allows you to integrate high-performance signal processing at the logic-level, on a PC platform, using high-end analog I/O with an accurate DDS or external clock timebase.

The card is delivered with the basic logic blocks needed to control the converters and the Omnibus interface, and VHDL source is provided for these units to allow users to integrate their algorithm. The VHDL source framework implements data flow to a FIFO, trigger control and Omnibus interface. In addition to the VHDL source files, a test bench and control files are included for Xilinx Foundation.

The CF module is the younger brother of our successful HSA module. The CF offers similar flexibility and the same conversion speed but at a much more affordable price. It is ideal for providing a logic solution to high-speed data acquisition and signal processing algorithm requiring a firmware approach. Applications that are possible include down-conversion/up-conversion, decimation, filtering, mixing, threshold detection and cropping, ultra high-speed servo, image pre-processing and automatic gain control (AGC).

The analog inputs are built around Analog Devices AD9226, 12-bit converters with up to 65MHz sampling. The analog chain consist of 50 ohm input, a low distortion amp, an optional programmable gain amp giving a range of –14dB to +34dB, followed by a 7th order low-pass filter into the A/D. The two's complement data from the converters clock into the FPGA that will process the data and buffer it to FIFO's prior to transfer to host. The size of the FIFO can be adjusted up to 1 Ksamples, and can be configured to interrupt the host board at programmable levels. Clocking is provided with an on-board, dual channel, 0-65MHz DDS with 0.01Hz resolution based on a stable 5ppm TCXO or an external clock source.

The analog outputs are Analog Devices AD9765, a 12-bit 65MSPS D/A, followed by a 7th order low-pass filter, an output buffer amp and a single-ended output matched to 50 ohms. The DAC's are fed by FIFO buffers and triggered by the on-board DDS or an external clock. The DAC FIFO levels are monitored in a FIFO_status register that can trigger interrupts to the host card.

Digital gain and offset correction are done in real-time in the FPGA for both input an output channels. A full calibration report ships with every module.

Software examples are provided for diagnostic testing and as example of peripheral usage. Experience programming FPGA's with the Xilinx Foundation tools in VHDL is required to create the specific functionality is required. Innovative Integration can be contracted for custom logic development.

Ordering Information

CF (without programmable gain amp)	80020-28
CF (with programmable gain amp)	80020-28A
SMB to BNC Cable	67021